

Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently amended) A semiconductor device comprising:

a semiconductor region comprising a source region, a drain region, a channel region, and a pair of regions between the channel region and the source and drain regions, said pair of regions formed of a same material as said channel region wherein each of said pair of regions has a first portion contiguous to the channel region and a second portion contiguous to the source or drain regions;

~~[[a gate]]~~ an insulating film formed adjacent to over said semiconductor region;

a first conductive layer vertically overlapped with the channel region and having the

~~[[gate]]~~ insulating film interposed therebetween; ~~[[and]]~~

a second conductive layer formed ~~adjacent to~~ over said first conductive layer;

a third conductive layer formed over said insulating film;

a fourth conductive layer formed over said third conductive layer;

an interlayer insulating film formed over said first conductive layer, said second conductive layer, said third conductive layer, and said fourth conductive layer;

at least one contact hole in said interlayer insulating film; and

a wiring connected to one of said source and drain regions;

wherein a width of the second conductive layer is narrower than that of the first conductive layer, ~~[[;]]~~

wherein the first conductive layer extends beyond side edges of the second conductive layer and extending portions of the first conductive layer overlap the first portions of said pair of regions while the second portions are not overlapped by said first conductive layer, and

~~wherein the semiconductor device forms a bottom-gate type transistor in which the first conductive layer and the second conductive layer are located below the semiconductor region~~

wherein a width of said third conductive layer is narrower than that of said fourth conductive layer,

wherein said fourth conductive layer extends beyond side edges of the third conductive layer, and

wherein said wiring overlaps with said third conductive layer and said fourth conductive layer.

2-43. (Cancelled)

44. (Currently amended) A semiconductor device comprising:

a semiconductor region comprising a source region, a drain region, a channel region, and a pair of regions between the channel region and the source and drain regions, said pair of regions formed of a same material as said channel region wherein each of said pair of regions has a first portion contiguous to the channel region and a second portion contiguous to the source or drain regions;

[[a gate]] an insulating film formed adjacent to over said semiconductor region;

a first conductive layer vertically overlapped with the channel region and having the

[[gate]] insulating film interposed therebetween; **[[and]]**

a second conductive layer formed adjacent to over said first conductive layer;

a third conductive layer formed over said insulating film;

a fourth conductive layer formed over said third conductive layer;

an interlayer insulating film formed over said first conductive layer, said second conductive layer, said third conductive layer, and said fourth conductive layer;

at least one contact hole in said interlayer insulating film; and

a wiring connected to one of said source and drain regions;

wherein a width of the second conductive layer is narrower than that of the first conductive layer, **[[;]]**

wherein the first conductive layer extends beyond side edges of the second conductive layer and extending portions of the first conductive layer overlap the first portions of said pair of regions while the second portions are not overlapped by said first conductive layer,

~~wherein the semiconductor device forms a bottom gate type transistor in which the first conductive layer and the second conductive layer are located below the semiconductor region,~~
and

wherein the first conductive layer and the second conductive layer are different materials,
wherein a width of said third conductive layer is narrower than that of said fourth conductive layer,

wherein said fourth conductive layer extends beyond side edges of the third conductive layer, and

wherein said wiring overlaps with said third conductive layer and said fourth conductive layer.

45. (Currently amended) A semiconductor device comprising:

a semiconductor region comprising a source region, a drain region, a channel region, and a pair of regions between the channel region and the source and drain regions, said pair of regions formed of a same material as said channel region wherein each of said pair of regions has a first portion contiguous to the channel region and a second portion contiguous to the source or drain regions;

~~[[a gate]]~~ an insulating film formed ~~adjacent to~~ over said semiconductor region;
a first conductive layer vertically overlapped with the channel region and having the ~~[[gate]]~~ insulating film interposed therebetween; ~~[[and]]~~

a second conductive layer formed ~~adjacent to~~ over said first conductive layer;
a third conductive layer formed over said insulating film;
a fourth conductive layer formed over said third conductive layer;
an interlayer insulating film formed over said first conductive layer, said second conductive layer, said third conductive layer, and said fourth conductive layer;

at least one contact hole in said interlayer insulating film; and

a wiring connected to one of said source and drain regions;

wherein a width of the second conductive layer is narrower than that of the first conductive layer, ~~[[;]]~~

wherein the second conductive layer extends beyond side edges of the conductive layer and extending portions of the second conductive layer overlap the first portions of said pair of regions while the second portions are not overlapped by said second conductive layer, and

~~wherein the semiconductor device forms a bottom gate type transistor in which the first conductive layer and the second conductive layer are located below the semiconductor region;~~

wherein a distance between the first portion and the source or drain region is larger than a thickness of the ~~[[first]]~~ second conductive layer,

wherein a width of said third conductive layer is narrower than that of said fourth conductive layer,

wherein said fourth conductive layer extends beyond side edges of the third conductive layer, and

wherein said wiring overlaps with said third conductive layer and said fourth conductive layer.

46-47. (Canceled).

48. (Currently amended) A semiconductor device comprising:

a semiconductor region comprising a source region, a drain region, a channel region formed on an insulating surface, and a pair of regions between the channel region and the source and drain regions, said pair of regions formed of a same material as said channel region wherein each of said pair of regions has a first portion contiguous to the channel region and a second portion contiguous to the source or drain regions;

~~[[a gate]]~~ an insulating film formed ~~adjacent to~~ over said semiconductor region;

a first conductive layer vertically overlapped with the channel region and having the ~~[[gate]]~~ insulating film interposed therebetween; ~~[[and]]~~

a second conductive layer formed ~~adjacent to~~ over said first conductive layer;
a third conductive layer formed over said insulating film;
a fourth conductive layer formed over said third conductive layer;
an interlayer insulating film formed over said first conductive layer, said second
conductive layer, said third conductive layer, and said fourth conductive layer;
at least one contact hole in said interlayer insulating film; and
a wiring connected to one of said source and drain regions;

wherein a width of the second conductive layer is narrower than that of the first conductive layer, ~~[[;]]~~

wherein the second conductive layer extends beyond side edges of the first conductive layer and extending portions of the second conductive layer overlap the first portions of said pair of regions while the second portions are not overlapped by said second conductive layer,

~~wherein the semiconductor device forms a bottom gate type transistor in which the first conductive layer and the second conductive layer are located below the semiconductor region,~~
and

wherein a distance between the first portion and the source or drain region is equal to or less than a thickness of the first conductive layer,

wherein a width of said third conductive layer is narrower than that of said fourth
conductive layer,

wherein said fourth conductive layer extends beyond side edges of the third conductive
layer, and

wherein said wiring overlaps with said third conductive layer and said fourth conductive
layer.

55. (Previously presented) A semiconductor device according to claim 1, wherein each of the first and second conductive layers comprises a material selected from the group consisting of molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt.

56. (Previously presented) A semiconductor device according to claim 44, wherein each of the first and second conductive layers comprises a material selected from the group consisting of molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt.

57. (Previously presented) A semiconductor device according to claim 45, wherein each of the first and second conductive layers comprises a material selected from the group consisting of molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt.

58-59. (Canceled).

60. (Previously presented) A semiconductor device according to claim 48, wherein each of the first and second conductive layers comprises a material selected from the group consisting of molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt.

61. (Currently amended) A semiconductor device according to claim 1, wherein a distance between the first portion and the source or drain region is ~~500 Å~~ 500 Å to ~~1000 Å~~ 1000 Å.

62. (Currently amended) A semiconductor device according to claim 44, wherein a distance between the first portion and the source or drain region is ~~500 Å~~ 500 Å to ~~1000 Å~~ 1000 Å.

63. (Currently amended) A semiconductor device according to claim 45, wherein a distance between the first portion and the source or drain region is ~~500 Å~~ 500 Å to ~~1000 Å~~ 1000 Å.

64-65. (Canceled)

66. (Currently amended) A semiconductor device according to claim 48, wherein a distance between the first portion and the source or drain region is ~~500 Å~~ 500 Å to ~~1000 Å~~ 1000 Å.

67. (Previously presented) A semiconductor device according to claim 1, wherein said insulating film comprises silicon oxide.

68. (Previously presented) A semiconductor device according to claim 44, wherein said insulating film comprises silicon oxide.

69. (Previously presented) A semiconductor device according to claim 45, wherein said insulating film comprises silicon oxide.

70-71. (Canceled)

72. (Previously presented) A semiconductor device according to claim 48, wherein said insulating film comprises silicon oxide.

73. (Previously presented) A semiconductor device according to claim 1, wherein said first conductive layer comprises tantalum and said second conductive layer comprises aluminum.

74. (Previously presented) A semiconductor device according to claim 44, wherein said first conductive layer comprises tantalum and said second conductive layer comprises aluminum.

75. (Previously presented) A semiconductor device according to claim 45, wherein said first conductive layer comprises tantalum and said second conductive layer comprises aluminum.

76-77. (Canceled)

78. (Previously presented) A semiconductor device according to claim 48, wherein said first conductive layer comprises tantalum and said second conductive layer comprises aluminum.

79. (Previously presented) A semiconductor device according to claim 1, wherein the semiconductor region comprises crystalline silicon.

80. (Previously presented) A semiconductor device according to claim 44, wherein the semiconductor film comprises crystalline silicon.

81. (Previously presented) A semiconductor device according to claim 45, wherein the semiconductor region comprises crystalline silicon.

82-83. (Canceled)

84. (Previously presented) A semiconductor device according to claim 48, wherein the semiconductor film comprises crystalline silicon.

85. (New) A semiconductor device according to claim 1, wherein a thickness of said second conductive film is 0.2 to 2 times greater than the thickness of said insulating film

86. (New) A semiconductor device according to claim 44, wherein a thickness of said second conductive film is 0.2 to 2 times greater than the thickness of said insulating film

87. (New) A semiconductor device according to claim 45, wherein a thickness of said second conductive film is 0.2 to 2 times greater than the thickness of said insulating film

88. (New) A semiconductor device according to claim 48, wherein a thickness of said second conductive film is 0.2 to 2 times greater than the thickness of said insulating film.

89. (New) A semiconductor device according to claim 1, wherein said first conductive layer and said second conductive layer are covered with an oxide film.

90. (New) A semiconductor device according to claim 44, wherein said first conductive layer and said second conductive layer are covered with an oxide film.

91. (New) A semiconductor device according to claim 45, wherein said first conductive layer and said second conductive layer are covered with an oxide film.

92. (New) A semiconductor device according to claim 48, wherein said first conductive layer and said second conductive layer are covered with an oxide film.